

**What is claimed is:**

*Sub A12*

1. A semiconductor device, comprising  
an I/O region formed on a chip and having at least an  
input/output pad;  
an active region formed on said chip;  
a plurality of logic circuits having either the same  
functions or different functions being mounted in said active  
region, and  
10 a selection circuit for selectively operating only one  
of said plurality of mounted logic circuits.

2. The semiconductor device according to claim 1, wherein  
said selection circuit includes a disconnecting section,  
15 and  
said disconnecting section is disconnected to allow  
permanent setting of an operable circuit.

*Sub B1*

3. The semiconductor device according to claim 2, wherein  
20 said disconnecting section includes a fuse.

*Sub A13*

4. The semiconductor device according to claim 1, wherein  
said selection circuit selects a logic circuit to be  
operated on the basis of a signal input supplied from the outside  
25 through said input/output pad.

5. The semiconductor device according to claim 1, wherein  
said selection circuit includes a transistor element  
connected in series with each said logic circuit between said  
30 logic circuit and a power terminal, and  
said transistor element selects a logic circuit to be  
operated on the basis of a signal input supplied from the outside

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through said input/output pad.